An Ultra Broad Band 300 W GaAs Power FET for W-CDMA Base Stations

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Abstract An ultra broad band 300 W power FET for W-CDMA base stations systems has been developed. This FET consists of four newly developed 260 mm total gate width (Wgt) chips fabricated with a quasi enhancement-mode (E-mode) structure. The broadband performance is obtained by means of multi-stage quarter wave length transformers, which are formed on high dielectric constant thin substrates. The developed FET demonstrated the performance of 300 W (54.8 dBm) saturated power and 11 dB linear gain at 2.15 GHz. In addition 0.2 dB power gain flatness was achieved across 180 MHz band width (at output power 47dBm). The group delay of this device was 2.14 nanosecond and the phase flatness was less than 0.35 degree between 2.11 and 2.17 GHz. This is the highest output power and widest bandwidth device ever reported.

I. Introduction

The final stage high power devices of W-CDMA system, which exhibit around 200 W output power have been reported. [1-5]. However, devices with over 300W are needed to increase the number of users and the variety of data communication services. The W-CDMA system uses the band width of 60 MHz, which is two to three times larger than current systems. The W-CDMA amplifier generally uses pre-distortion or feed-forward techniques for noise cancellation. Therefore wide band performance is required for this application. In this paper, we report on the 300 W push-pull FET with ultra wide band performance.

II. Chip Structure and Design

A highly Si doped GaAs channel layer, AlGaAs Schottky layer, and a WSi/Au T-shaped gate were employed. The highly doped channel brings a high transconductance, which significantly improves the gain, power-added-efficiency (PAE) performance and linearity of the device as reported in [1], [6]. The GaAs wafer was thinned to 28 μm and the gold on the backside was plated up to 40 μm. Besides thinning a GaAs wafer, employing a larger channel area design is also effective to reduce the thermal resistance, especially in a case of 300W output FET with 260 mm gate width per chip. The width of the chip was limited to 4 mm because of practical requirements, for example chip warping in soldering. Therefor, a longer unit gate width (Wgu) is preferable in a view of the thermal resistance, and the Wgu determined to 930 μm. Figure 1 is a photograph of 80W output chip. Each cells has 20-fingers with 14-cells combined in chip.

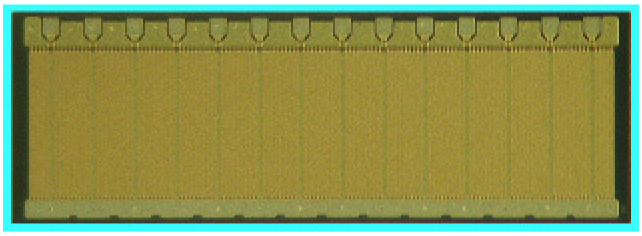

Fig. 1 Photograph of 80W chip

Ⅲ. Circuit Design

Figure 2 shows the internal view of a developed 300W GaAs FET. The package size is 34.0 x 17.4 mm. and a pair of chips are combined with in-phase divider and combiner and the two sets of the combined chips are assembled in a push-pull configuration in the package. We estimated the design target impedance by using source and load-pull measurement of unit chip cell. The optimum source and load impedances were about 0.5 ohm and 1.6 ohm. We employed the three-stage input circuit and the two-stage output circuit. The Input and output matching circuits need to be fabricated with the proper transfer ratio by reason of bandwidth performance.

A transmission line's impedance of gate side

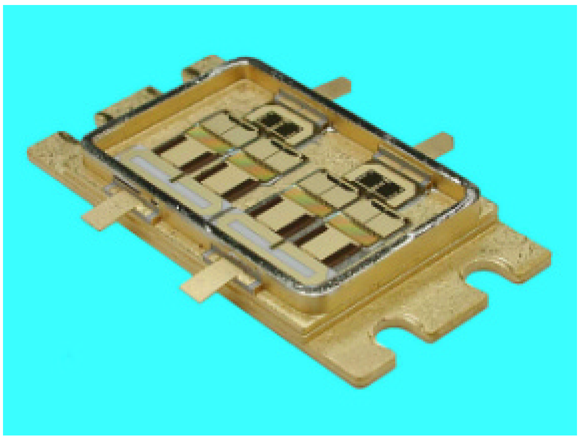

Fig. 2 internal view of a 300W GaAs FET

must be very low in particular. Therefore we use 0.1mm thickness and dielectric constant of 140 substrate.

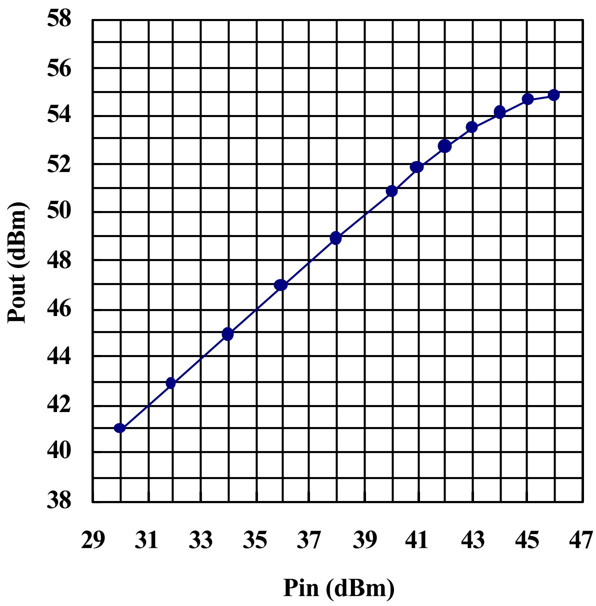

Fig. 3 Output power vs. input power.

@ Vds=12V, IDS(DC)=6.0A, f=2.15GHz

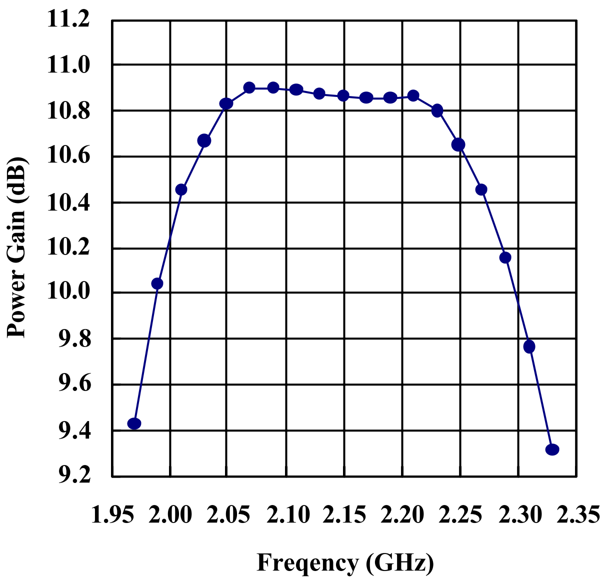

Fig. 4 Power gain vs. frequency

@ Vds=12V, IDS(DC)=6.0A, Pout=47dBm

IV. RF Performance

Figure 3 shows the measured output power of the push-pull FET at 2.15 GHz. A saturation power of 54.8 dBm (300 W) was achieved with an associated linear gain of 11 dB at 2.15 GHz. Figure 4 shows the measured power gain of 47 dBm output power, the FET exhibits a flat bandwidth of 180 MHz which is defined by the gain flatness within 0.2 dB from the peak point. If the criteria of 0.5 dB gain flatness is applied, the bandwidth is 260 MHz. Figure 5 shows the adjacent channel leakage power ratio (ACPR) measured by using the W-CDMA modulation signal. An ACPR level of –35 dBc with a power-added efficiency of 25 % was obtained at an output power of 47 dBm. The feed-forward or pre-distortion is commonly used to cancel ACP of W-CDMA system. And, these distortion chancellor systems affect the group delay and phase flatness of devices. Figure 6 shows the group delay and phase flatness of developed device. The group delay was 2.14 nano seconds and the phase flatness was less than 0.35 degree between 2.11 and 2.17 GHz. The FET also showed a thermal resistance of 0.4 deg-C/W, which was measured by delta VGS method.

V. Conclusion

An ultra broadband 300 W power FET has been developed successfully. The FET exhibits an associated linear gain of 11 dB at 2.15 GHz. This is the highest output power and widest bandwidth performance using GaAs FET technology ever reported. An ACPR level of –35 dBc with a power-added efficiency of 25 % was obtained at an output power of 47 dBm. The developed FET is a promising device for use in the W-CDMA base stations.

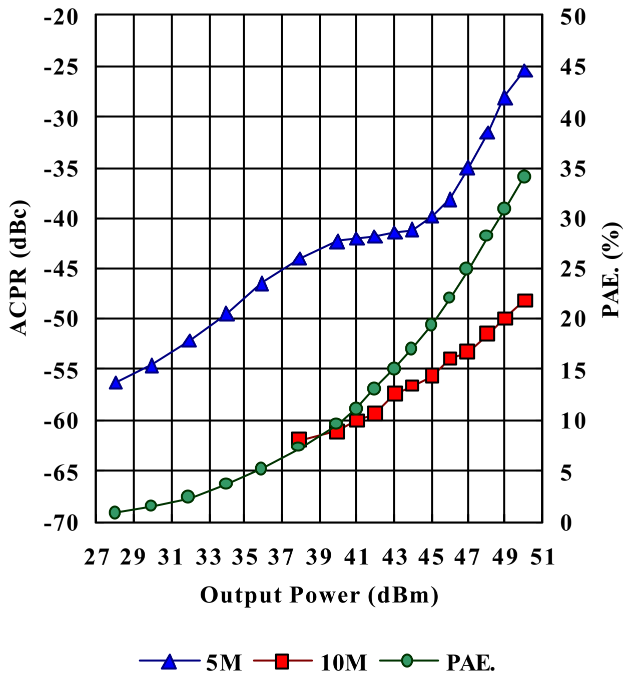

Fig.5 ACPR and power-added efficiency vs. output power@ Vds=12V, IDS(DC)=6.0A, f=2.15GHz

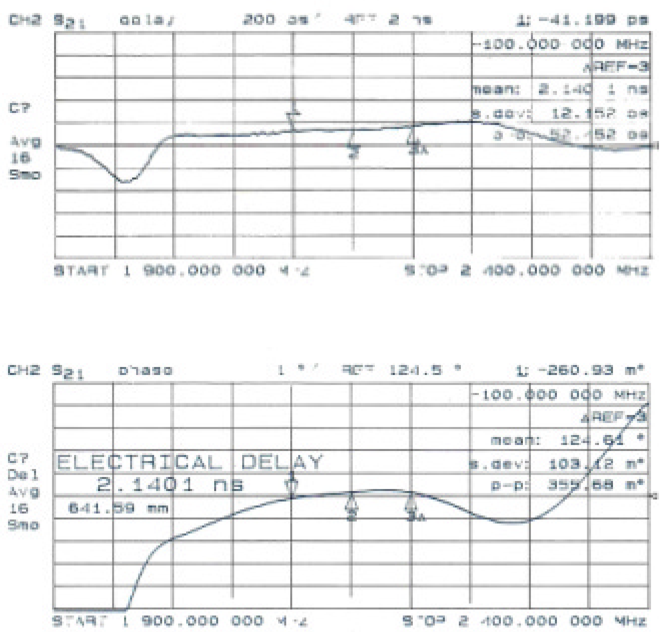

Fig. 6 Group delay and phase flatness @ Vds=12V, IDS(DC)=6.0A

VI. Acknowledgement

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VII. References

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